NEW NEURAL PLL ARCHITECTURE

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Abstract: A PLL or phase-locked loop is a control system that creates an output signal whose phase is related to the phase-locked loop and represents controlled input signal. The goal of this research is to first investigate the functioning of new PLL neural networks and then, in the research section, explore an approach involving the extraction of neural symmetrical voltage components. The architectural characteristics of phase-locked loops (PLLs) typically include capture and lock ranges, bandwidth, and transient response. The new neural PLL architecture offers several advantages, such as low noise performance, reduced silicon area, and compatibility with low supply voltages. However, it may also present disadvantages, including hardware dependency and potential design complexity compared to traditional PLL architectures. Evaluating these factors is crucial, depending on the specific needs of the application.

In this paper, we present the scientific research included in the experimental part where we investigate the performance of the proposed neural PLL, for which experimental comparisons with the conventional PLL in a distorted reference frame are necessary. Structural columns or structural circles will be used for graphic display.

The following research methods and techniques will be applied: instruments, basic methods and data processing procedures - if they are foreseen. What makes this work a scientific research work is a descriptive method that will be used.

To better understand how PLLs work, we propose an original three-phase neural approach for components of the system's phase and symmetry. The quality of the electricity can be assessed and managed with this framework. Our study shows that the full neural architecture may be applied to three-phase power systems because it is based on DSP supplies. Additionally, we present the performance of the PLL system in a three-phase power supply context. Different regulators, such as PI and RST based on phase logic, are incorporated into the PLL scheme. The results suggest that the neural PLL could make a significant contribution in applications where the quality and efficiency of three-phase power systems are essential.

Keywords: Neural Phase-Locked Loop (PLL), electroenergetic system, neural network, neural architecture

INTRODUCTION

A controlled system known as a phase-locked loop (PLL) produces an output signal that is both phase and frequency synced with an input reference signal. As integrated circuits have advanced, the PLL has emerged as a crucial component for numerous applications, including signal processing boards, three-phase power systems, and contemporary communication systems [1].

PLLs play a crucial role in power systems. Among the uses are drive control, harmonic current detection, unbalance compensation in three-phase systems, and sinusoidal inverter control.

The proposed neural phase-locked loop (NPLL) employs a neural algorithm capable of decoding time-coded information and converting it into a rate code. This advance suggests improvements in the ability to efficiently track and process signals, leveraging neural networks for better performance in systems that rely on phase-locked loops. Recently, dedicated PLLs have been designed, comprising a three-phase PLL designed to calculate the phase angle of direct sequence components and the system frequency. APF methods have effectively employed this strategy in situations involving severely distorted voltage [1].

The subject of this research is the application of new neural PLLs as symmetrical components to estimate system frequency and the phase angle of direct sequence components, which are used in APF schemes.

The goal of the research is to first investigate the functioning of the new PLL neural networks, includ-

ing their characteristics, advantages, and disadvantages. In the research phase, the focus is on the extraction of neural symmetrical voltage components, neural phase detection techniques, and functional tasks that are decomposed and approximated using Adaline neural networks are used. The complete neural architecture is applied to a three-phase power supply system and implemented on a digital signal processor (DSP).

Characteristics of Pll

Architecture characteristics of Phase Locked Loops (PLLs) typically include capture and lock ranges, bandwidth, and transient response. The capture range is generally smaller than the lock range, which defines how well the PLL can stabilize the output frequency against changes in the reference signal. PLLs are widely used every day in many areas of high frequency system design.

According to its various operating principles and methods, a phase-locked loop (PLL) refers to a control system that can generate output signals according to certain rules. By comparing the different operating principles, it can be determined that the basic principle of PLL is to realign the phase of the input signal. This mode of PLL operation is significantly different from traditional output signals, which is achieved by adjusting the local frequency of the generated signal, which in turn adjusts its phase [1].

Feedback control in a PLL circuit

In a phase-locked loop (PLL), the phase and frequency of the output signal are aligned with the input signal through a phase- and frequency-locking mechanism. This process is achieved by a closed-loop control system, which uses feedback to continuously adjust the phase and frequency of the local oscillator to match those of the input signal, thereby maintaining system stability. The feedback control in a PLL is based on phase detection, where a phase detector generates an error signal proportional to the phase difference between the input and local oscillator signals. This error signal is then processed through a low-pass filter, which eliminates high-frequency components, before being fed back to the local oscillator. As the local oscillator frequency adjusts, the phase difference decreases, and the error signal diminishes. This iterative process continues until the phases and frequencies of the output signal are synchronized with those of the input signal.

Clock distortion generation and elimination

Clock skew is a timing error that can occur in digital systems due to various factors. Before we explain how PLLs lead to clock skew, here are some common reasons why this happens:

- A delay in the transmission of the clock signal through the transmission line can lead to clock distortion. When clock signals travel through a transmission line, various delays can occur due to factors such as the length of the transmission line, the impedance of the line, and depending on what kind of material is used to make the line [2]. This delay can cause clock signals to arrive at different times and ultimately result in clock skew.
- Temperature and voltage variations can also cause clock skew in digital systems. The delay of the clock signal can vary with temperature and voltage changes, which can lead to clock distortion.Treperenje sata je još jedan faktor koji može uzrokovati iskrivljenje sata. Treperenje sata je varijacija u vremenu signala sata zbog nastanka šuma ili smetnji. Ovo takođe može prouzrokovati odstupanje dolaska signala do sata.

However, PLL can solve the clock skew problem in digital systems. It can generate a clock signal that is synchronized with an input clock signal or a reference clock signal, and then eliminate any timing differences between these signals. To do this, the PLL compares the phase and frequency of the input clock signal or reference clock signals with phase and frequency [3]. This comparison is performed by a phase detector, which generates signal errors proportional to the phase and frequency difference between the signals. By using feedback control to adjust the frequency and phase of the locally generated clock signal, the PLL will be able to eliminate any timing differences between the input clock or clock signal. This ensures that the clock signals in the digital system are properly synchronized [4].

Frequency multiplication

A frequency multiplier in a PLL can take an input signal and produce an output signal whose frequency

is a multiple of the input frequency. It can be implemented using a variety of circuit techniques, such as doublers, triplers, or higher-order multipliers. In the context of a PLL, a frequency multiplier is usually implemented using a nonlinear device, such as a diode, transistor, or mixer, that performs a multiplication operation on the input signal. The multiplication factor (M) of the frequency multiplier determines how many times the frequency of the locally generated clock signal is increased. For example, if the input clock signal has a frequency of 10 MHz and the frequency multiplication factor is 4, the output clock signal would have a frequency of 40 MHz.

Components of PLL

Figure 1 illustrates the fundamental circuit of the PLL, highlighting its unique characteristics, operational principle, and structural design. Through detailed investigation and analysis, it was determined that this configuration offers strong resistance to external disturbances and fluctuations, thereby ensuring the stability of the entire system.

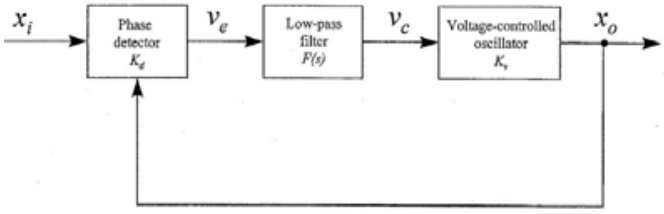

Figure 1. *Basic PLL circuit*

Phase detector

The phase detector plays a crucial role in the system. As a central component in the control process, its primary function is to detect signal errors, ensuring the system maintains high accuracy and precision at all times. This prevents performance degradation caused by excessive errors. For instance, the square PD (phase detector) signal is commonly utilized in PLL design. The characteristics of the square signal PD have a linear type over the detection phase, while the triangular PD and the sawtooth PD have different types of phase detection [5].

Low pass filter

Among all the structural components of the PLL, there is a (one) very important one that plays a role in eliminating noise and ensuring the stability of the output signal current of the entire system. The low-pass filter is a very important component, so it is necessary to select relevant parameters and a reasonable working environment during selection and design. The output of the phase detector, which is proportional to the phase error, contains high frequency components that need to be filtered out before they are used to tune the voltage controlled oscillator (VCO). If these high-frequency components are not filtered, they will cause instability of the VCO output signal, which then results in frequency instability [6].

Voltage controlled oscillator

A voltage controlled oscillator (VCO) plays a role in generating output signals with a frequency that is synchronized with the reference input signal. By applying voltage control to the resonant circuit, the frequency of the output signal can be adjusted. A VCO works by generating a sinusoidal waveform, with a frequency that is a function of the input voltage applied to it. The frequency range of the output signal is typically determined by components in the circuit resonance, such as inductors and capacitors [7].

NEW ARCHITECTURES USED IN PLL ARCHITECTURE

Over the years, various new architectures have been proposed for the design of phase-locked loops (PLLs) to overcome the challenges faced by traditional PLLs and to improve their performance. Here are some examples of new PLL architectures:

(1) Fractional-N PLL: Fractional-N PLL is a modified version of the traditional integer-N PLL that allows the PLL to generate frequencies that are not integer multiples of the reference frequency.

(2) All-digital PLL: An all-digital PLL (ADPLL) uses only digital circuitry, eliminating the need for analog components such as VCOs and filters [8]. ADPLLs offer several advantages over traditional PLLs, including better scalability, lower power consumption, and higher noise immunity.

(3) Bang-Bang PLL: Bang-Bang PLL uses digital phase detector and switched capacitor filter to achieve high frequency resolution and low phase noise. This architecture is suitable for low power applications and is used in frequency synthesizers for wireless communication systems.

These new PLL architectures contributed to the advancement of PLL technology and enabled the de-

sign of PLLs with improved performance, scalability, and energy efficiency [9].

Advanced loop filters and improved phase detectors in PLL design

Loop filters and phase detectors are critical components of a Phase Locked Loop (PLL) because they determine the stability, noise performance, and lock time of the PLL. Over the years, several advanced loop filters and improved phase detectors have been developed to address the challenges faced by traditional PLLs and improve their performance [10]. Here are some examples:

(1) Proportional-Integral (PI) Loop Filters: PI loop filters are commonly used in PLLs due to their simplicity and good stability characteristics. However, they can have poor transient response and phase noise. To solve this, advanced PI loop filters have been developed that use non-linear elements such as RC filters, resonators or active elements to improve the performance of the PLL.

(2) Phase charge detectors: Phase charge detectors are widely used in PLLs because of their simplicity and good performance. However, they can be prone to errors, which can cause phase noise and thus limit the lock range of the PLL. To solve this problem, improve this phase, detectors using current mirror techniques, self-calibration circuits or multilayer quantization to reduce displacement errors have been developed [11].

(3) Digital phase detectors: Digital phase detectors offer several advantages over analog phase detectors, including better accuracy, programmability, and noise performance. But they can be affected by delay errors and quantization noise [12]. To solve this problem, digital phase has been improved and phase detectors have been developed that use delay-locked loops, dynamic latches, or multiphase clocking to improve their performance. These advanced loop filters and improved phase detectors have contributed to the development of PLLs and significantly improve performance, stability and noise characteristics, making PLLs more suitable for a wide range of applications in communication systems, radars, instrumentation and other fields.

After describing the new neural PLLs in the research section we will explore how the IPT-based PLL works. This approach is derived as a lead in a new formulation of current powers used by Adalin's neural network[13]. Adaline is a straightforward, easily learned design that is effective at online linear connection estimation. This served as a powerful incentive for the use of digital technologies in PLL implementation. As a result, the novel neural PLL and its improved digital signal processor (DSP) implementation are ideally suited for a full neural APF scheme and can meet real-time limitations [14].

Advantages and Disadvantages of the new Neural PLL Architecture

The new neural PLL (Phase-Locked Loop) architecture offers several advantages, including low noise performance, reduced silicon area, and compatibility with low supply voltages. However, it can also have disadvantages such as hardware dependency and potential complexity in design compared to traditional PLL architectures. It is important to evaluate these factors based on the specific needs of the application.

Advantages

The most popular PLL architecture is the fully differential PLL [15]. This architecture offers several advantages in terms of low noise performance, reduced silicon area and compatibility with low supply voltages. In addition, it is well suited to meet the demanding requirements imposed by modern wireless devices. Another popular architecture is the digital PLL, which can be either fully digital or include a VCKSO for low jitter requirements [16]. A digital PLL overcomes the limitation of hard-to-change design parameters when the PCB is mounted. Commonly used for clock recovery and cleanup in transmission media. Another proposed architecture is a modified architecture that allows full monolithic integration [17]. This design employs a switched capacitor filter in place of a passive filter and a phase frequency detector that operates at a 90 degree phase shift [17]. It achieves the same performance as conventional solutions with a significantly lower capacity.

The new neural PLL (Phase-Locked Loop) offers several advantages, including improved flexibility in handling different types of data, improved self-learning capabilities, and better performance even with sparse data. This approach also simplifies un-

derstanding how neural networks produce outputs, making artificial intelligence more understandable.

Disadvantages

Disadvantages of the new phase-locked neural loops (PLLs) may include the following:

- Complexity: Neural PLLs can be more complex to design and implement compared to traditional PLLs, making them more difficult to understand and use effectively.
- Computational overhead: These can require significant computing resources for training and inference, leading to increased latency and power consumption.
- Overfitting: As with many machine learning models, there is a risk of overfitting the training data, which can lead to poor generalization in real-life scenarios.
- Black-box nature: The "black-box" nature of neural networks can make it difficult to interpret how decisions are made, complicating debugging and optimization efforts.

Always consider verifying information based on context and specific applications.

NEW ARCHITECTURE OF NEURAL PLL

We will go over how to keep an eye on a measured three-phase voltage system's fundamental frequency. The two stages of the suggested method, which is depicted in Figure 2, are the extraction of symmetrical voltage components and the current phase identification algorithm. The problem that leads to the initial signal decomposition that is, current powers and voltages is formalized for each stage. In any case, we demonstrate that Adaline neural networks can be used to learn these phrases. As a result, the entire strategy is quite flexible and can accommodate for shifting factors.

Method of extraction of symmetrical neural components

IPT serves as the foundation for the symmetric component extraction concept. This theory states that the pk-powers are computed and that their AC and DC terms are instantly separated. The direct voltage components are then determined by converting the DC-terms to the current reference frame, as seen in Figure 3. The instantaneous powers in IPT are computed using the αβ–frame.

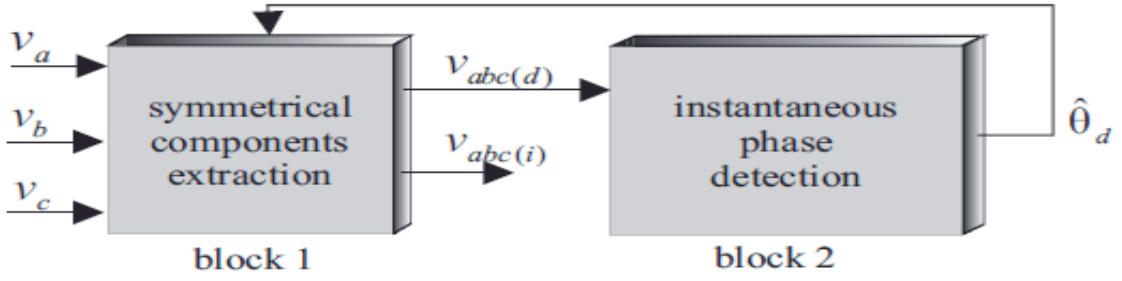

Figure 2. *The basic principle of PLL with two different functional blocks*

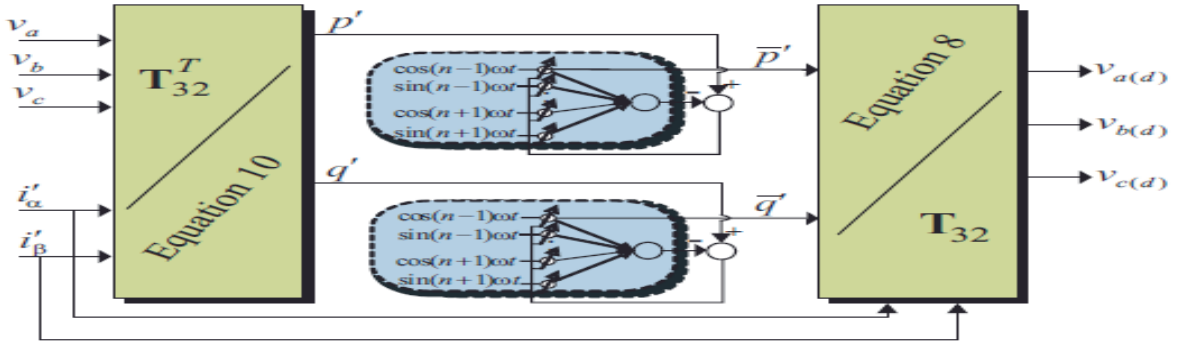

Figure 3. *Symmetrical component extraction system*

The supply voltage in the αβ-frame can be deduced to be:

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{1}{(i_\alpha^2 + i_\beta^2)} \begin{bmatrix} i_\alpha & i_\beta \\ i_\beta & -i_\alpha \end{bmatrix} \begin{bmatrix} p \\ q \end{bmatrix}. \tag{7}$$

Formula (7) is a general formulation that enables the determination of the αβ−voltage. This expression can be used to determine the basic components of the DC voltage using the currents obtained from the direct basic system and the DC-term of the connected powers, ie:

$$\begin{bmatrix} v_{\alpha(d)} \\ v_{\beta(d)} \end{bmatrix} = \frac{1}{(i'^2_\alpha + i'^2_\beta)} \begin{bmatrix} i'_\alpha & i'_\beta \\ i'_\beta & -i'_\alpha \end{bmatrix} \begin{bmatrix} \bar{p}' \\ \bar{q}' \end{bmatrix}. \tag{8}$$

The currents i′α and i′β correspond to basic ic direct currents in the αβ-frame with a phase of zero and an amplitude of unity:

$$\begin{bmatrix} i'_\alpha \\ i'_\beta \end{bmatrix} = \begin{bmatrix} \cos\omega t \\ \sin\omega t \end{bmatrix}. \tag{9}$$

The imaginary powers p' and k' are likewise computed using these currents. These powers are based on observed voltages $vabc$ and i_α^' and i_β^' currents, but they have no actual physical meaning.

$$\begin{bmatrix} p' \\ q' \end{bmatrix} = \begin{bmatrix} v_\alpha i'_\alpha + v_\beta i'_\beta \\ v_\beta i'_\alpha - v_\alpha i'_\beta \end{bmatrix} \tag{10}$$

The following is a detailed description of the fake active power p':

$$\begin{aligned} p' &= v_\alpha i'_\alpha + v_\beta i'_\beta \\ &= \sum_{n=1}^{N} \begin{bmatrix} \cos(n-1)\omega t & \sin(n-1)\omega t \end{bmatrix} \begin{bmatrix} 3V_{dn}\cos\phi_{n(d)} \\ -3V_{dn}\sin\phi_{n(d)} \end{bmatrix} \\ &+ \sum_{n=1}^{N} \begin{bmatrix} \cos(n+1)\omega t & \sin(n+1)\omega t \end{bmatrix} \begin{bmatrix} -3V_{in}\cos\phi_{n(i)} \\ +3V_{in}\sin\phi_{n(i)} \end{bmatrix} \end{aligned} \tag{11}$$

Formula (11) is a sum of harmonic components that can be rewritten by a linearly separable equation:

$$y = x^T W \tag{12}$$

za: $$\mathrm{x} = \mathrm{x}(t) = \begin{bmatrix} \cos(n-1)\omega t \\ \sin(n-1)\omega t \\ \cos(n+1)\omega t \\ \sin(n+1)\omega t \end{bmatrix}; \mathrm{w} = \begin{bmatrix} 3V_{dn}\cos\phi_{n(d)} \\ -3V_{dn}\sin\phi_{n(d)} \\ -3V_{in}\cos\phi_{n(i)} \\ 3V_{in}\sin\phi_{n(i)} \end{bmatrix} \tag{13}$$

Adalin's neural network learns and approximates formula (11). Adaline's input vector is x, which consists of multiples of the fundamental component in the form of synthesized sinusoidal signals, if y in (12) is its output. Adaline's output is compared to an example, which is the intended value obtained with simulated currents and measured voltages v_abc during operation (11). Adaline is based on supervised learning. Error ε=p′−i corrects Adaline's weight v while sampling using an optimal LMS (least mean square) learning technique [9]. The weights of Ada, v, are compelled to converge under these circumstances. The power amplitudes resulting from direct voltages at frequency nω and currents determined by formula (9), after training, are represented by elements v. The three-phase system's fundamental forward voltages, v_(abc(d)), are determined using.

$$\begin{bmatrix} i'_\alpha \\ i'_\beta \end{bmatrix} = \begin{bmatrix} \cos(\omega t) \\ -\sin(\omega t) \end{bmatrix}. \quad (14)$$

The zero-sequence voltage components $vabc(0)$ can be inferred from the fundamental forward and inverse voltage components $vabc(d)$ and $vabc(i)$. A phase detection method can also use them to get a real-time approximation of the power system frequency.

EXPERIMENTAL RESULTS

To evaluate the performance of the proposed neural PLL, experimental comparisons with a conventional PLL in a distorted reference frame are essential. The primary experimental setup is shown in Figure 4. A synchronous generator (SG), driven by a DC motor, supplies the three-phase power distribution system. By adjusting the DC motor's current, the frequency of the three-phase voltages feeding the system can be varied. Figure 5 demonstrates how harmonic distortions affect these voltages.

A DSP dSPACE board (DS1104) with a sampling time Ts = 0.3 ms is used to implement the neural voltage component extraction algorithm and several PLLs. A traditional PLL with a PI controller and the following parameters—Kp = 0,3 and Ki = 0,02—is used to compare the suggested approaches.

The experimental section of the paper details the performance of the proposed neural PLL and its comparison with the conventional PLL in a distorted reference frame.

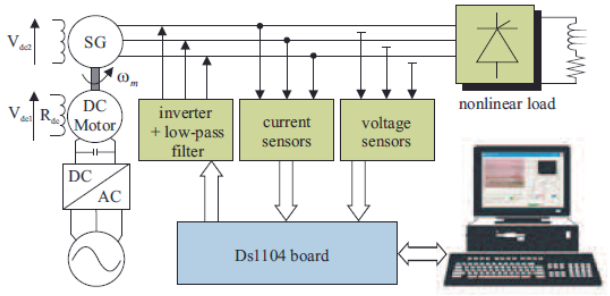

Figure 4. *An experimental platform*

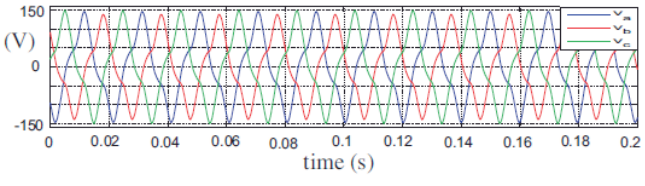

Figure 5. *Waveforms of the supply voltage of a three-phase power system*

Extraction of the inverse voltage component

The inverse voltage components were also extracted by the proposed methods. The results are shown in Figure 6, where the neural symmetric component extraction method outperforms the traditional PLL with LPF and PI controller in terms of speed. Figure 7's spectral representation is used to assess the performance. The basic component is estimated using a neural method with a 1% error and a traditional PLL with a 4% error.

Figure 6 displays the frequency estimation outcomes of the three techniques. In terms of durability, performance, and speed, the neural PLL offers superior estimation compared to the conventional PLL and the suggested instantaneous phase detection approach. The amount of computational time required by any approach has a significant impact on its performance. There are non-negligible processing costs involved in transforming between distinct reference frames (from the ABC-frame to the αβ-frame, and vice versa). Furthermore, temporal delays are a feature of the LPF and PI controller systems. Conversely, the neural PLL has the ability to react instantly. Adaline uses a linear regression function for learning, which converges quickly and iteratively modifies the weights to produce output that is correct and current.

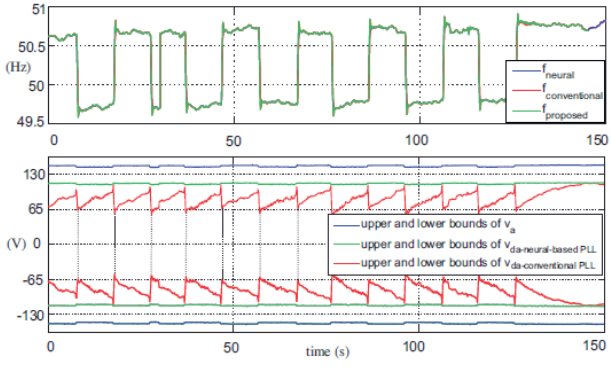

Figure 6. *Frequency monitoring and extraction of direct voltage components*

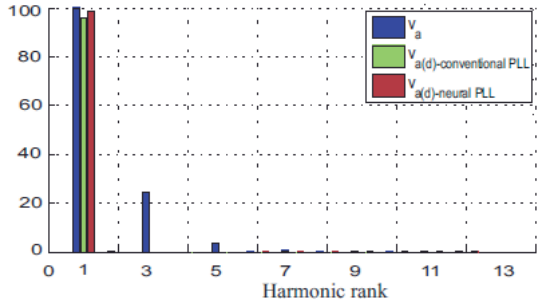

Figure 7. *The frequency spectrum of the DC voltage component*

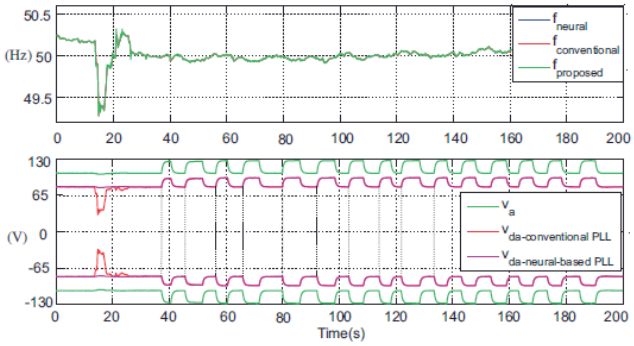

Figure 8. *Estimation of frequency and direct voltage with amplitude variations*

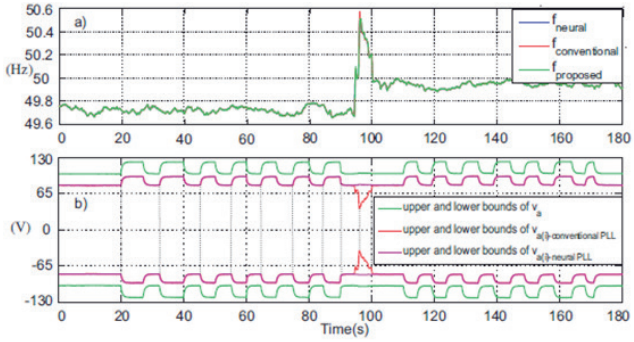

Figure 9. *Estimation of frequency and inverse voltage with amplitude variations*

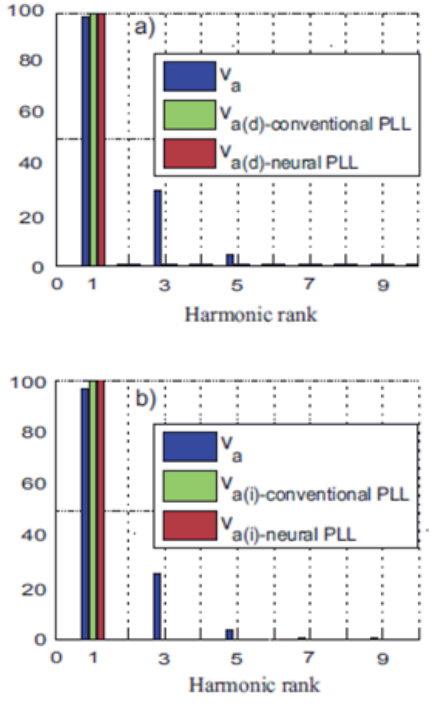

Figure 10. *Frequency spectrum of the estimated voltages: (a) the spectrum of the direct voltage component, (b) the spectrum of the inverse voltage component*

Neural symmetric components and frequency estimation with voltage drops

Previous experiments used a three-phase constant-amplitude voltage system. In the following experiments, the frequency and three-phase voltages are changed. The voltage amplitude changes The frequency shifts quickly at t = 13 s and fluctuates slightly about 50 Hz.

Evaluating the suggested approaches' resilience under these circumstances is the goal. Figure 8 displays frequency and voltages. For a single phase, voltages are solely depicted by their outlines. Va estimates are provided using both the traditional PLL and the neural symmetric component extraction technique. When the frequency varies significantly, the forward voltage component predicted by the traditional PLL is nearly identical to the estimate achieved with the neural PLL. In contrast to a typical PLL, which requires a few seconds to get an accurate voltage estimate, the neural symmetric component estimator may provide a rapid and precise voltage value instantly in the event of a sudden shift in frequency. In essence, when the frequency is steady, there is no need for the PI controller that is included in a traditional PLL. Conversely, the PI controller causes a time delay because it effectively attempts to cancel out the frequency estimate inaccuracy. The extraction of the inverse voltage components, as shown in Figure 9, is subject to the same remarks. The neural PLL, with its responsiveness and learning capabilities, is the most accurate estimator under voltage and frequency variations, provided that the frequency estimations are acceptable with the methods being studied.

The use of a PI (Proportional-Integral) controller is a key component in control systems for regulating process variables. It improves upon simple proportional control by eliminating steady-state error through the integral component. This ensures a better control of processes that require a consistent output over time. However, PI controllers can introduce overshoot and oscillation if not properly tuned. Alternatives to PI controllers include PID (Proportional-Integral-Derivative) controllers, which adds a derivative component to enhance stability and response time, and advanced control strategies such as adaptive control or fuzzy logic controllers that can deal with more complex systems. Make sure to double-check any technical specifics or implementation details on PI controllers as they can vary widely, based on application.

CONCLUSION

In conclusion, a phase-locked loop (PLL) is a control system designed to generate output signals based on specific principles, primarily by aligning the phase of an input signal. This paper introduces a novel neural PLL architecture that offers significant advantages, such as low noise performance, reduced silicon area, and compatibility with low supply voltages. We describe a three-phase neural approach for estimating phase and symmetrical components, utilizing fictitious expressions of active and reactive powers to train two Adaline estimators, which calculate forward and inverse voltage components. A phase detection method is then applied to these voltages, accurately determining the frequency.

The findings of our scientific research and experimental section of the work confirm (to us) the significant advantages of the new neural PLL architecture, which offers significant advantages, such as low noise performance, reduced silicon area and compatibility with low voltages compared to the conventional PLL architecture.

The trial results demonstrate the effectiveness of this approach, showing that the neural method reliably extracts primary voltage components and estimates the phase of a time-varying three-phase power system under conditions such as voltage dips, random noise, and harmonics. This proposed approach proves suitable for real-time harmonic current compensation in active power filtering systems. The entire neural architecture, implemented on a digital signal processor (DSP), is applied within a three-phase power supply system. The PLL plays a crucial role in power systems, with applications in drive control, harmonic current detection, unbalance compensation in three-phase systems, sinusoidal inverter control, and beyond.

Furthermore, the proposed neural PLL architecture provides a promising direction for future developments in power system control, particularly in enhancing the efficiency and stability of renewable energy integration, smart grids, and other advanced power electronics applications.

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